

FIG. 1

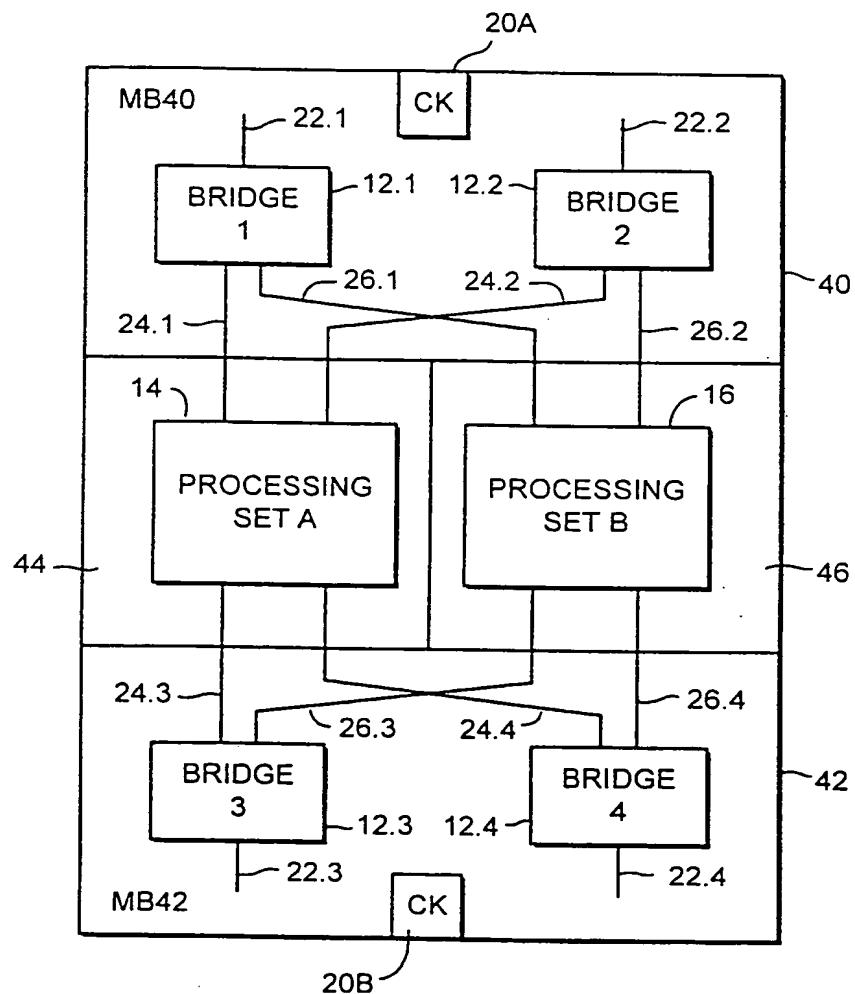


FIG. 2

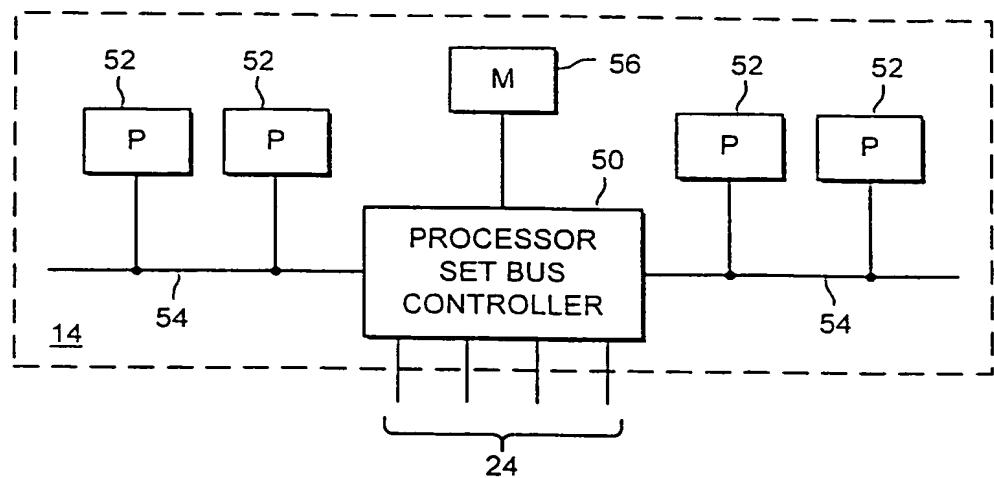


FIG. 3

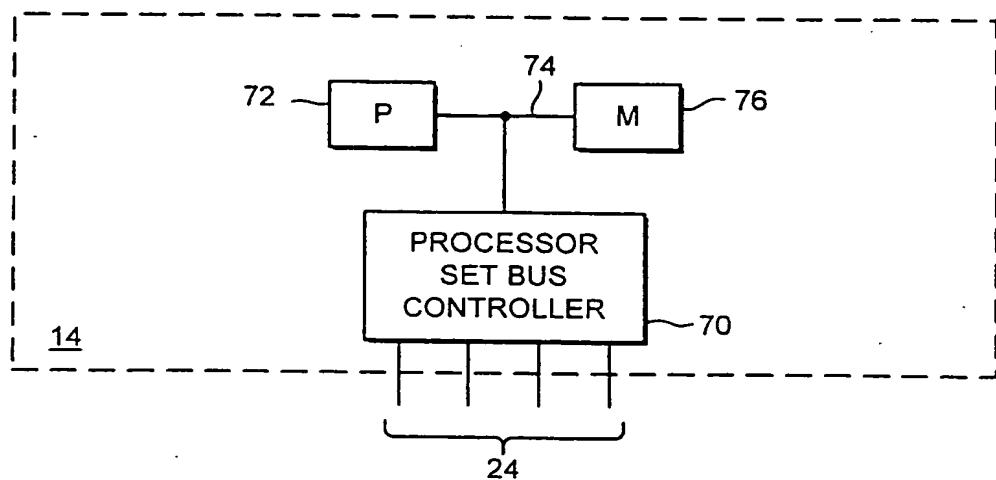


FIG. 4

126 SRAM  
110 BRIDGE REGISTERS  
90 STORAGE CONTROL LOGIC  
82 D BUS INTERFACE  
88 BRIDGE CONTROL LOGIC  
84 PA BUS INTERFACE  
24 PB BUS INTERFACE  
26  
21

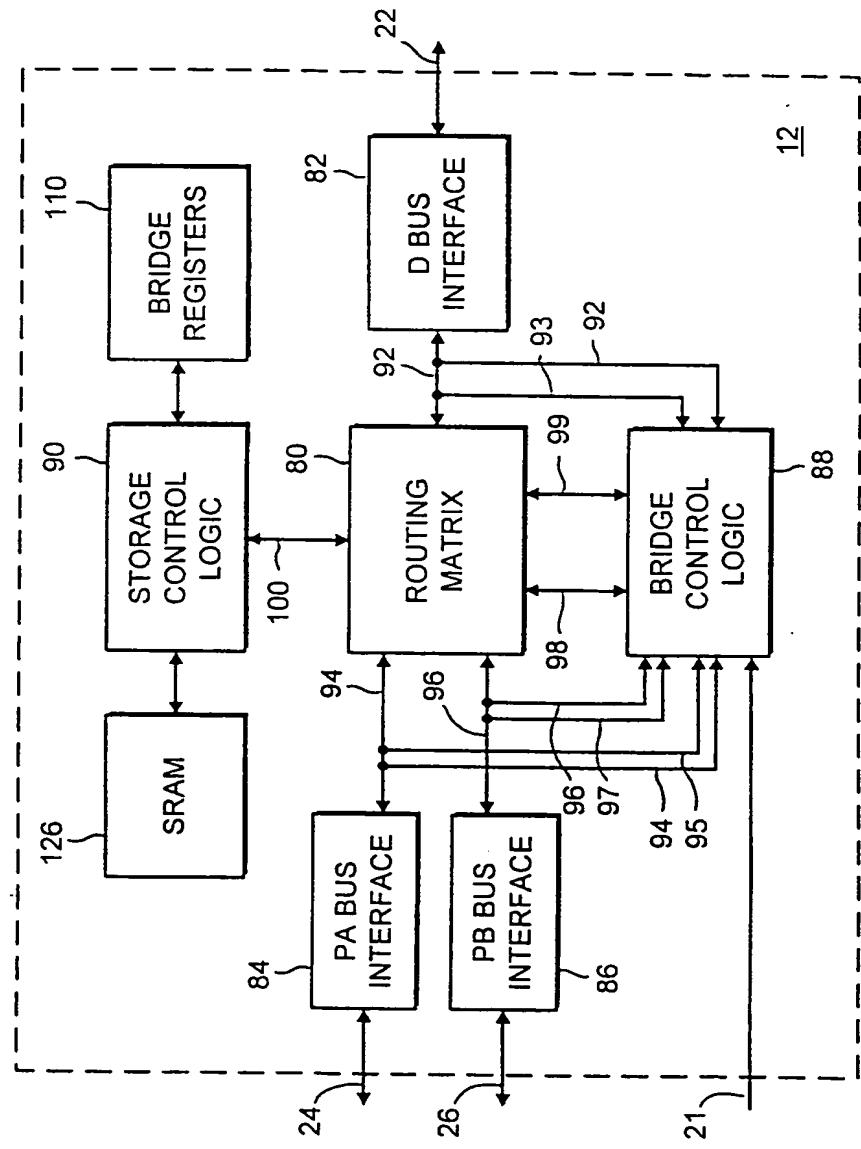


FIG. 5

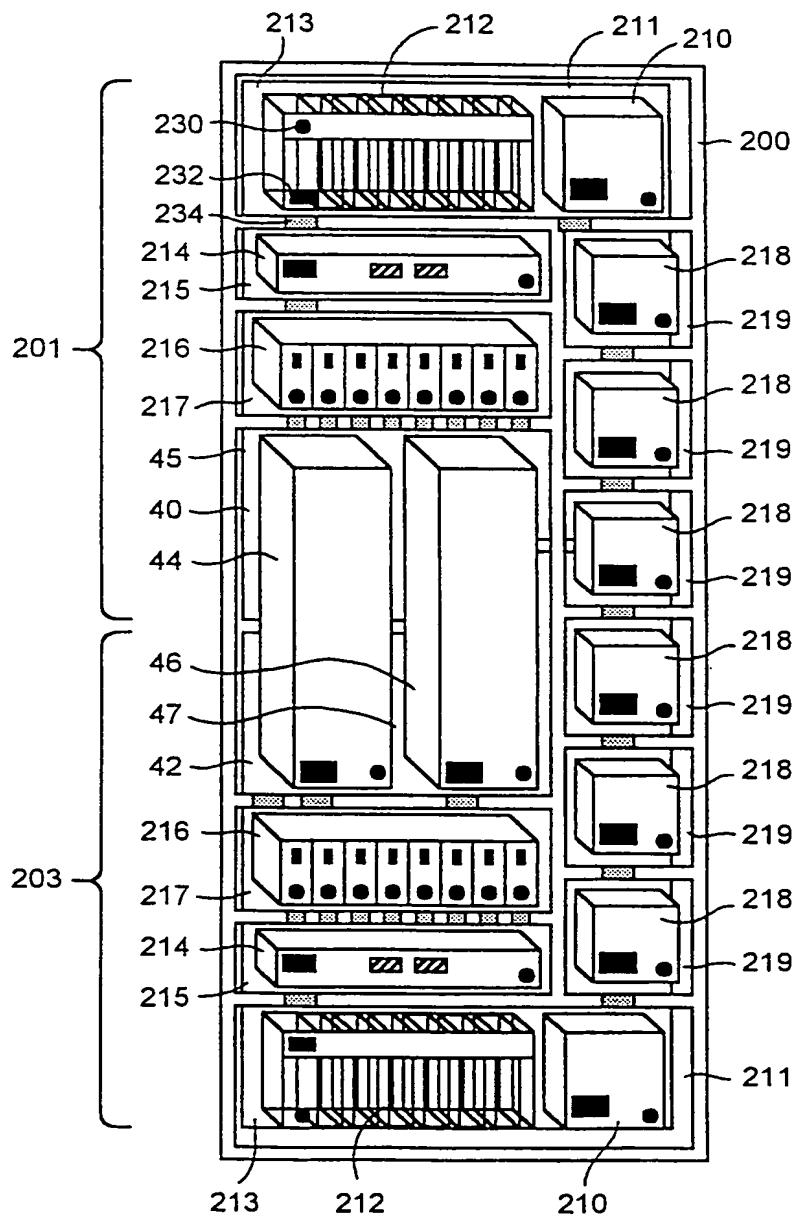


FIG. 6

IBM PC/AT Compatible Computer System

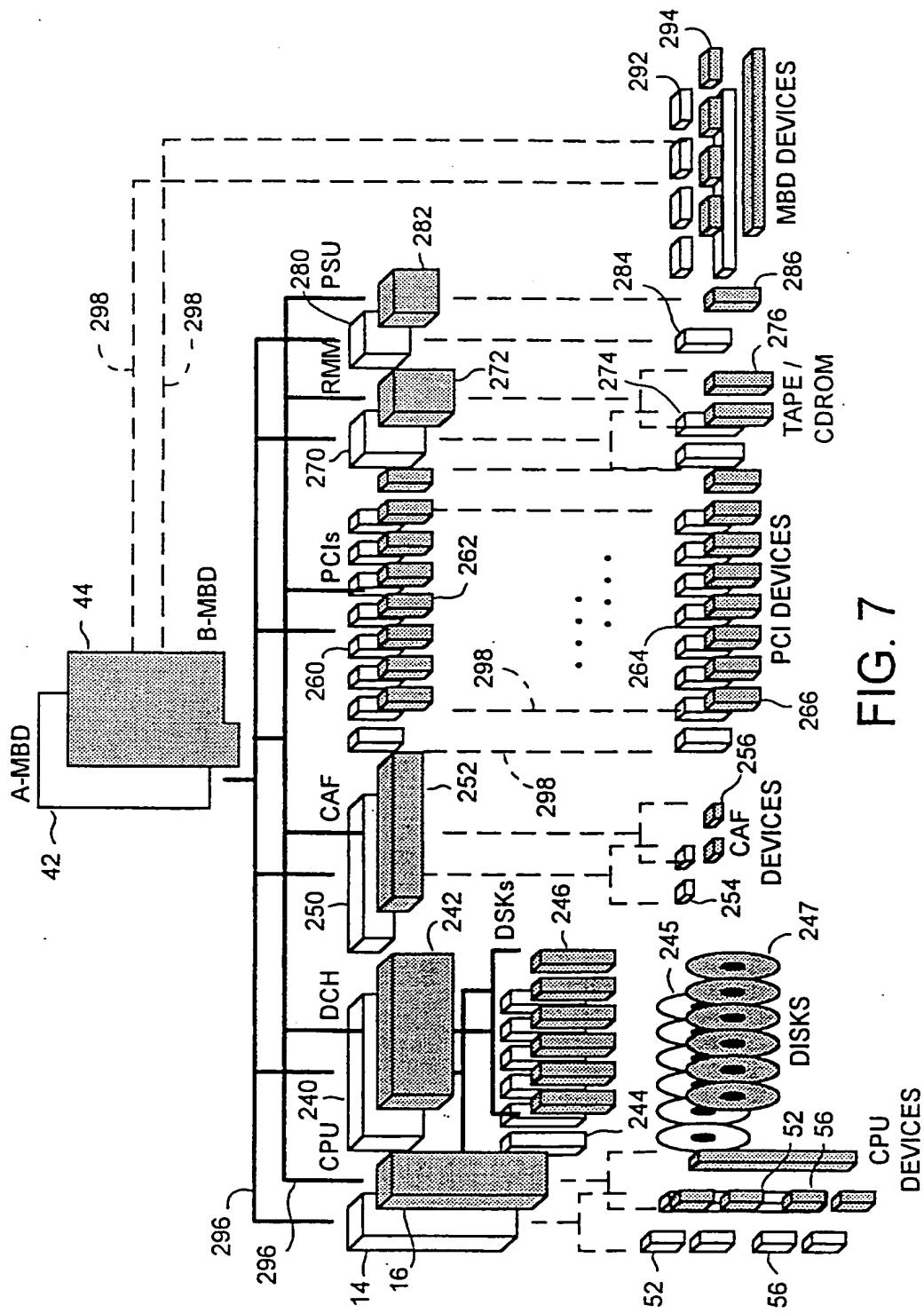


FIG. 7

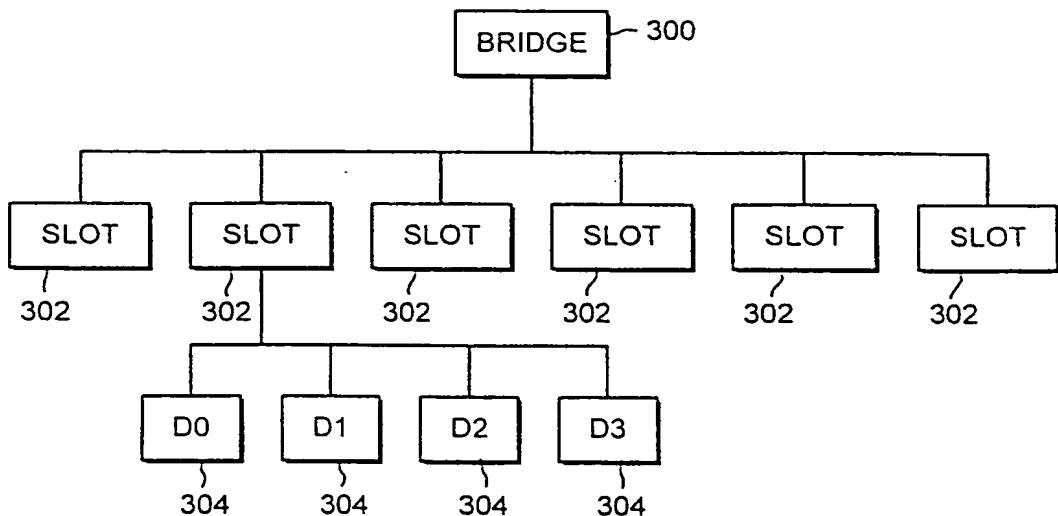


FIG. 8

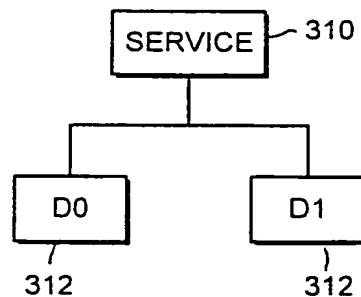


FIG. 9

P U B L I C D O C U M E N T • C O M P U T E R S

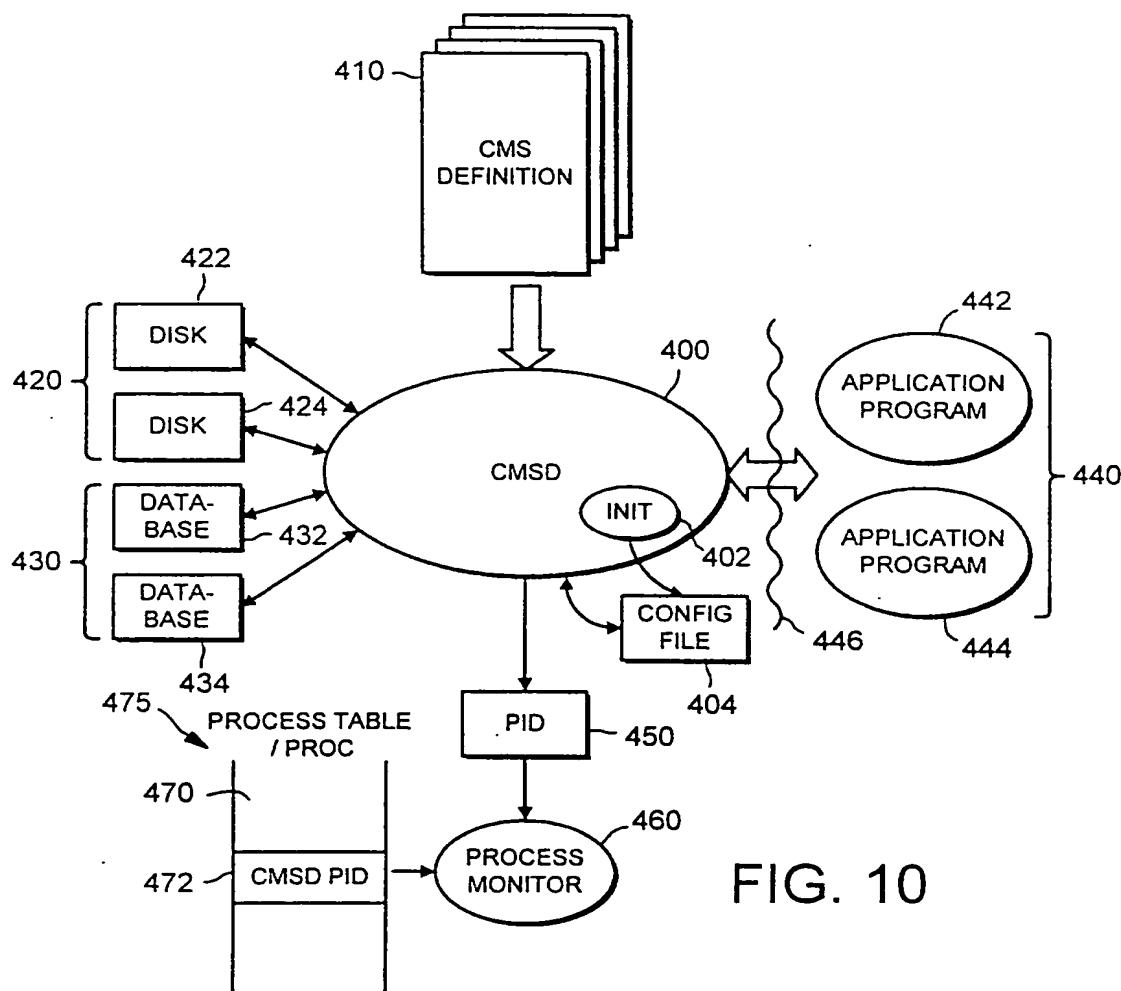


FIG. 10

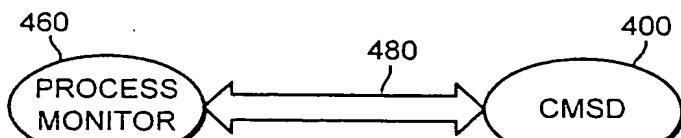


FIG. 11

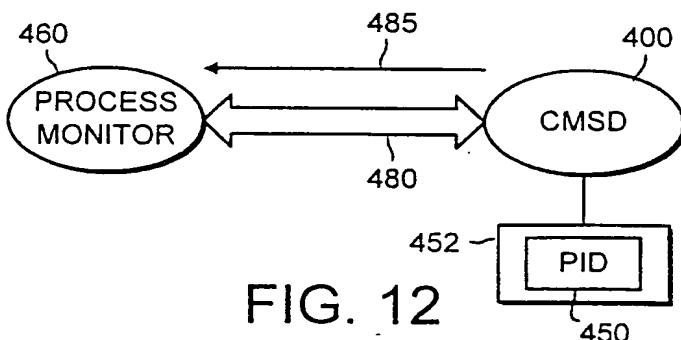


FIG. 12

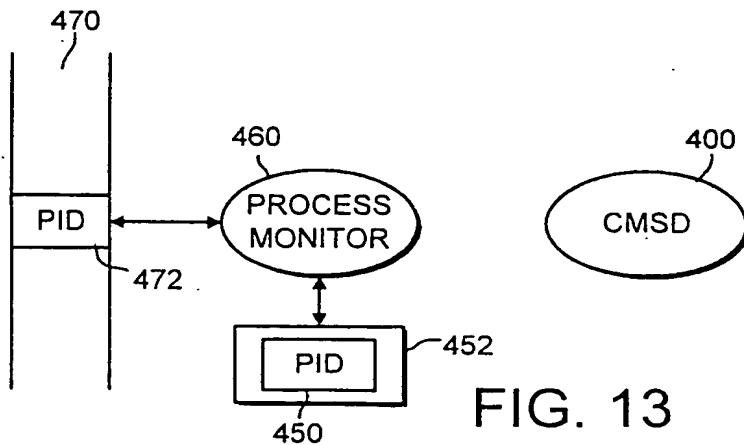


FIG. 13

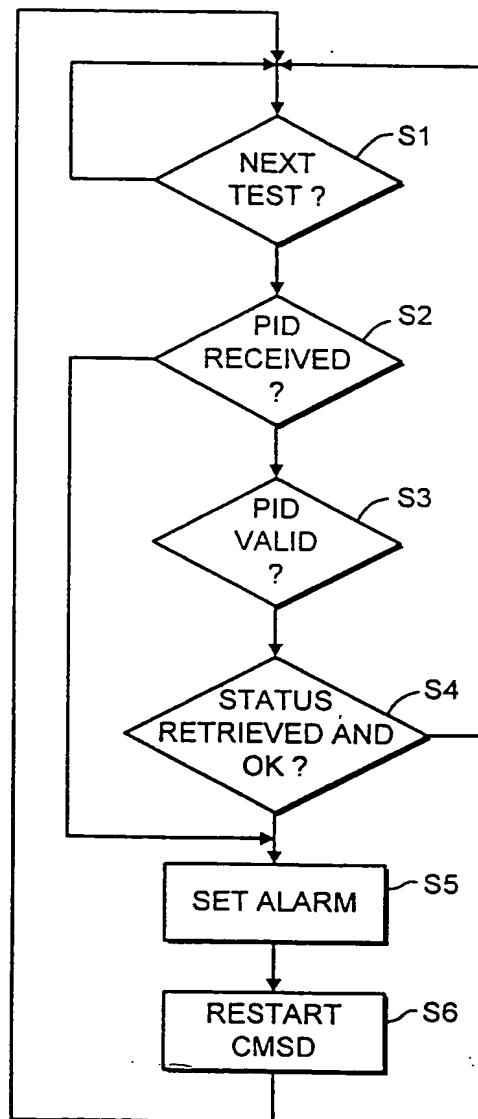


FIG. 14

100-000000000000000000000000000000

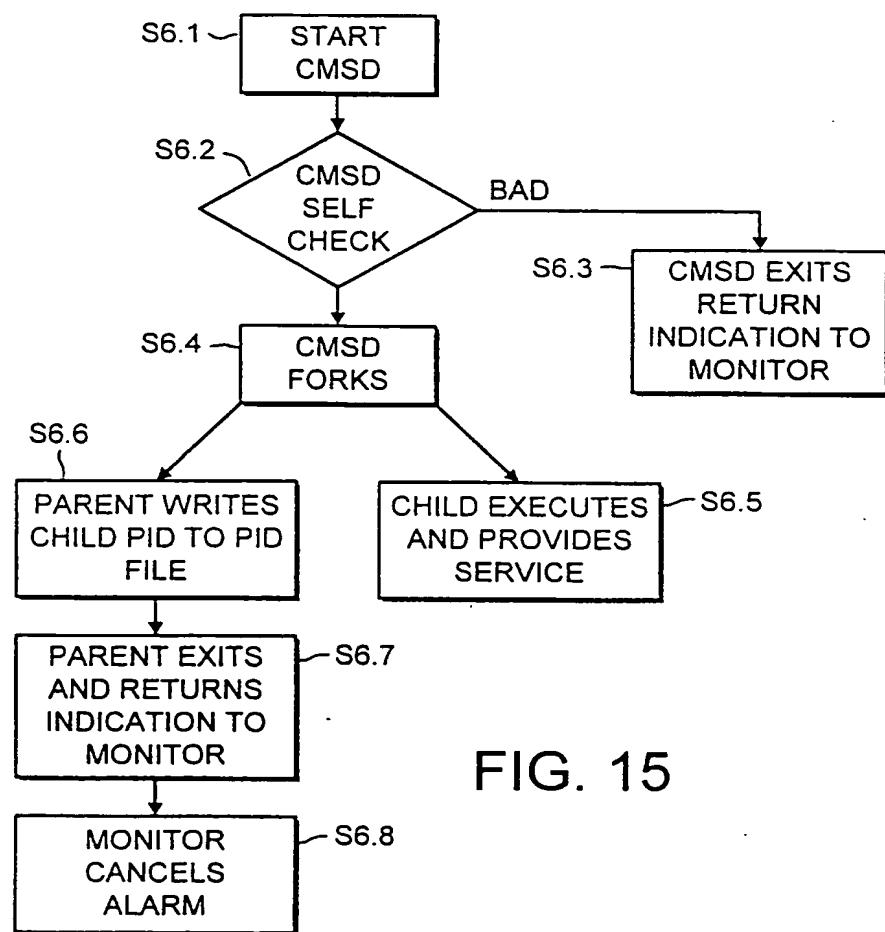


FIG. 15

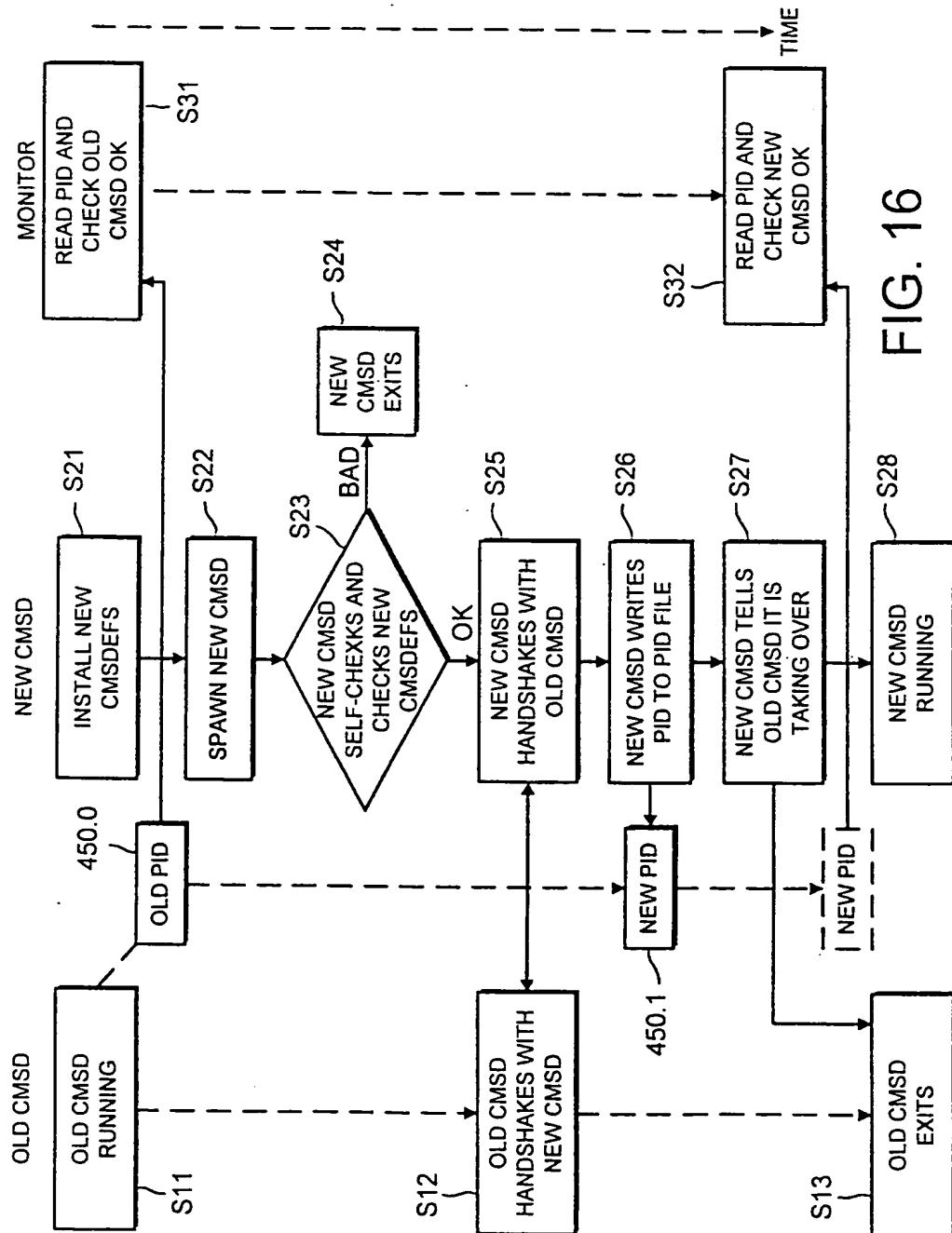


FIG. 16

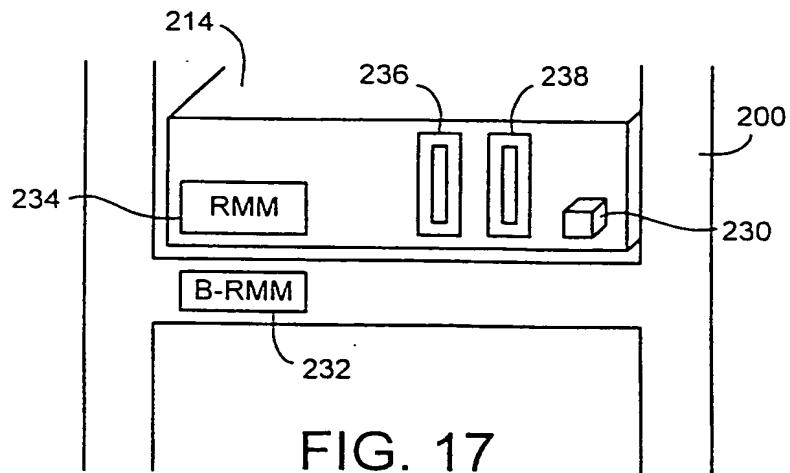


FIG. 17

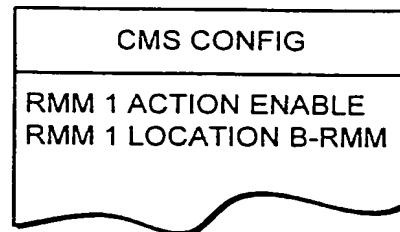


FIG. 18

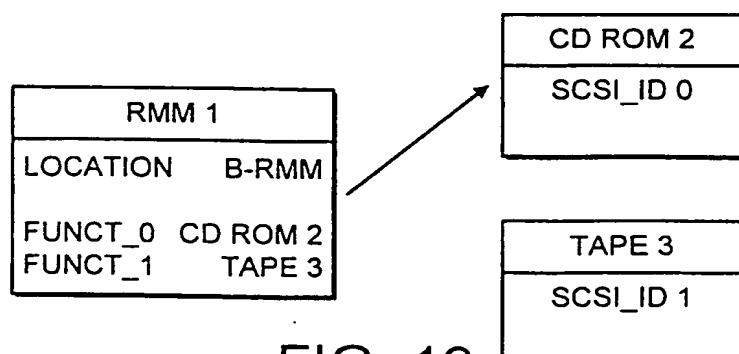


FIG. 19

P R E P A R E D F O R C O M M U N I C A T I O N S

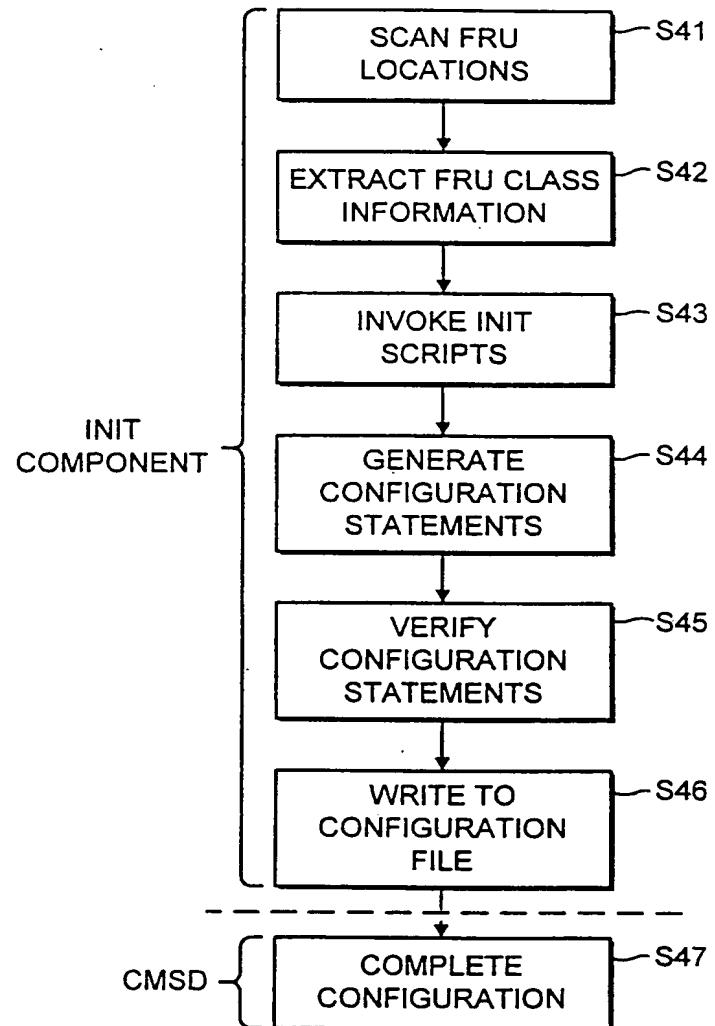


FIG. 20